What is claimed is:

1. A semiconductor component having a first layer (10) of a first type of conductivity having a top side and a bottom side, the top side being covered by a second layer (30) of a second type of conductivity, and a third layer (20) being situated on the bottom side,
wherein the first layer has areas (40, 50) of different thickness due to at least one depression (60) produced in the top side.

2. The semiconductor component according to Claim 1,
wherein the at least one depression is designed as a pit having a rectangular cross section.

3. The semiconductor component according to Claim 1 or 2,
wherein at least one quarter of the bottom side borders first areas (40) which do not have any depressions.

4. The semiconductor component according to one of the preceding claims,
wherein at least half the area of the bottom side borders second areas (50) having depressions.

5. The semiconductor component according to one of the preceding claims,
wherein an edge area is formed by second areas (40) where there are no depressions.

6. The semiconductor component according to one of the preceding claims,
wherein the second layer (30) is strongly doped.

7. The semiconductor component according to one of the preceding claims,
wherein the third layer (20) is of the first type of conductivity and is highly doped.

8. The semiconductor component according to Claims 6 and 7,
wherein the first layer and the third layer are provided with metallic coatings.

9. A method of manufacturing semiconductor components,
wherein depressions are produced in a wafer of a first type of conductivity, in another step both sides of the wafer are covered with doping atoms and a diffusion process is carried out, and in another step the wafer is divided into individual chips so that each chip has at least one depression (60) in its internal area (70).

10. The method according to Claim 9,
wherein the depressions are designed as pits having a rectangular cross section.

11. The method according to Claim 9 or 10,
wherein metal layers are applied to both sides of the wafer before dividing the wafer.

12. The method according to Claim 9, 10 or 11,
wherein the wafer is divided in areas (40) of the wafer where no depressions have been produced.

13. The method according to one of Claims 9 through 12,
wherein a dopant of a second type of conductivity is used in covering the top side.

14. The method according to one of Claims 9 through 13,
wherein a dopant of the first type of conductivity is used in covering the bottom side.

15. The method according to Claims 11, 13 and 14,
wherein the metal layers are applied to the first layer and the third layer.